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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,489	04/28/2005	Torayuki Tsukada	10921.313USWO	4098

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,489	TSUKADA ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 20 July 2007 have been entered.

Terminal Disclaimer

2. The terminal disclaimer filed on 20 July 2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of patent 7,129,814 or applications 10/517941 and 10/553044 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1- 7** are rejected under 35 U.S.C. 102(b) as being anticipated by Tsunoda (US 5,339,068).

5. Regarding claims **1-3 and 5-7**, Tsunoda discloses in Fig 15 a chip resistor comprising a chip resistor body having a front surface (top), a rear surface (bottom) provided at an interval in a thickness direction, a pair of side surfaces (Fig 14) extending in a length direction at an interval in a width direction, and a pair of end surfaces provided at an interval in the length direction; a plurality of electrodes (116) provided in series on the rear surface of the resistor body at intervals in the length direction and

also removed from edges of the rear surface in the fixed direction (116 removed from surface by 111 and 14); a solid layer metal coating layer (18) covering a respective one of the electrodes and a respective one of the end surfaces; a first insulation layer (14) covering regions between the plurality of electrodes on the front surface and the rear surface of the resistor, a second insulation layer (14) covering the pair of side surfaces of the resistor body, and a third insulation layer (14) covering the front surface of the resistor body, wherein the first through third insulation layers are made of an identical material; wherein each of the electrodes (116) and the metal coating layer (18) overlap a portion of the first insulation layer, said portion of the first insulation layer being inserted between the metal coating layer and the rear surface of the resistor body, the metal coating layer extending beyond the respective electrode into direct contact with the first insulation layer.

6. Regarding claim **4**, Tsunoda discloses the resistor of claim 2, wherein each of the electrode (116) has a greater thickness (col 9 ln than the first insulation layer (14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims **8 and 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali (EP 0 326 212) and Tsunoda.

Caporali discloses in Fig 1 a manufacturing method for chip resistors, each of which comprises: a chip resistor body having a front surface, a rear surface provided at an interval in a thickness direction, a pair of side surfaces extending in a length direction at an interval in a width direction, and a pair of end surfaces provided at an interval in the length direction; a plurality of electrodes (3) provided in a series on the rear surface of the resistor body at intervals in the length direction; a first and third insulation layer (2) covering a region between the plurality of electrodes on the front and rear surfaces of the resistor body, the method comprising the steps of:

producing a resistor aggregate (Fig 1D) shaped into a bar, the resistor aggregate having a rear face provided with a multiplicity of electrodes (3), the multiplicity of electrodes being arranged at intervals in a longitudinal direction of the resistor aggregate, regions between the multiplicity of electrodes on the rear face are covered with a first insulation layer (2); and dividing the resistor aggregate into a plurality of chip resistors (Fig 1E) having protruding resistor side faces (Fig 1D item 1 exposed) by

cutting the resistor aggregate in a plurality of locations in the longitudinal direction of the resistor aggregate.

Caporali does not specify forming a second insulation layer covering the pair of side faces of the resistor material, a metal coating layer covering a respective one of the electrodes and a respective one of the end surfaces, wherein each of the electrodes and the metal coating layer overlap a portion of the first insulation layer, said portion of the first insulation layer being inserted between the metal coating layer and the rear surface of the resistor body, the metal coating layer extending beyond the respective electrode into direct contact with the first insulation layer.

Tsunoda teaches forming an insulation layer surrounding the resistor material, even on the pair of side faces, to prevent the plated electrodes from contacting the resistor material, and to improve the heat resistance of the resistor without an increase in resistance value fluctuations (col 2 ln 47-55). Electrodes and metal coating layer (Fig 15 items 116 and 18) are formed to overlap a portion of the insulation layer and into direct contact with the insulation layer to improve the soldering heat resistance (col 5 ln 32-42 and col 5 ln 53-66). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Tsunoda in the method of Caporali to prevent the plated electrodes from contacting the resistor material and to improve the heat resistance of the resistor without an increase in resistance value fluctuations.

10. Claims **9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali and Tsunoda as applied to claim 8 above, and further in view of Doi (US

5,450,055). Caporali and Tsunoda teach the method of claim 8, wherein an insulation layer is formed on the pair of side surfaces of each resistor aggregate, but do not specify providing a pattern-formed insulation layer and a conductive layer serving as the electrodes on one surface (rear surface) of a resistor material plate, and then dividing the resistor material plate into a plurality of resistor aggregate.

Doi teaches a method of manufacturing chip resistors where a patterned insulated substrate has an electrode layer and a resistor layer formed thereon, and is then divided into bar-form resistor material (col 2 ln 30-44). The process is used because it allows formation of accurate chip resistors in a smooth supply tube for automatic mounting (col 1 ln 67- col 2 ln 9). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Doi in the method of Caporali and Tsunoda in order to form accurate resistors for automatic mounting.

11. Claims **13-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Caporali, Tsunoda and Kobayashi (US 6,955,942).

Caporali discloses in Fig 1 a manufacturing method for chip resistors, each of which comprises: a chip resistor body having a front surface, a rear surface provided at an interval in a thickness direction, a pair of side surfaces extending in a length direction at an interval in a width direction, and a pair of end surfaces provided at an interval in the length direction; a plurality of electrodes (3) provided in a series on the rear surface of the resistor body at intervals in the length direction; a first and third insulation layer

(2) covering a region between the plurality of electrodes on the front and rear surfaces of the resistor body, the method comprising the steps of:

producing a plurality of resistor aggregate (Fig 1D) in which a multiplicity of electrodes (3) is provided on a rear surface of the bar portions arranged at intervals in a length direction of the resistor material and being formed by a plating process after formation of the insulator layers (col 2 ln 1-3), and regions between the plurality of electrodes on the front and rear surface are covered with first and third insulation layers (2); and dividing the resistor aggregate into a plurality of chip resistors (Fig 1E) having protruding resistor side faces (Fig 1D item 1 exposed) by cutting the resistor aggregate in a plurality of locations in a length direction thereof. Caporali does not specify forming a second insulation layer covering the pair of side faces of the resistor material.

Tsunoda teaches forming an insulation layer surrounding the resistor material, even on the pair of side faces, to prevent the plated electrodes from contacting the resistor material, and to improve the heat resistance of the resistor without an increase in resistance value fluctuations (col 2 ln 47-55). Electrodes and metal coating layer (Fig 15 items 116 and 18) are formed to overlap a portion of the insulation layer and into direct contact with the insulation layer to improve the soldering heat resistance (col 5 ln 32-42 and col 5 ln 53-66). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Tsunoda in the method of Caporali to prevent the plated electrodes from contacting the resistor material and to improve the heat resistance of the resistor without an increase in resistance value fluctuations.

Caporali and Tsunoda do not specify preparing a conductive frame with plate-form portion on which the resistors are formed, or that the frame is rotated to form the second insulator layer.

Kobayashi teaches in Fig 6B a frame for chip resistors, serving as a starting material with supporting functions (col 3 ln 22-25) constituted by a conductive member comprising a plurality of plate-form portions extending in a fixed direction, each plate-form portion having a front surface, a rear surface, and a pair of side faces, and a support portion for supporting the plurality of plate-forms, wherein a connecting portion between each of the plate-form portions and the support portion is formed narrower than the plate-form portion and wherein the support portion has a frame shape, and each of two end portions in a length direction of each of the plate-form portions is supported on the support portion via the connecting portion. Kobayashi also teaches that it is well known in the art to rotate the frame during processing in order to work on each orthogonal angle (col 13 ln 10-20). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Kobayashi in the method of Caporali and Tsunoda in order to have a starting material that could also provide support for the chip resistors.

Response to Arguments

12. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner
Art Unit 2814

John C Ingham
Examiner
Art Unit 2814

/J. C. I./